www.ktubtechquestions.com

Course code	Course Name	L-T-P-Credits	Year of Introduction
IT365	Computer Architecture & Parallel Processing	3-0-0-3	2016

Prerequisite: Nil

Course Objectives

- To understand issues and techniques in improving performance of processors
- To understand the concepts of pipelining
- To familiarize with the properties of superscalar processors
- To understand the multiprocessor systems, multi core systems and the concept of cache coherence

Syllabus

Classes of parallelism and parallel architecture, computer architecture- design issues, Performance measurements, quantitative principles of computer design, Instruction level parallelism -concepts and challenges, Data dependencies and hazards, Basic compiler techniques for exposing ILP.Dynamic Scheduling- Tomasulo's approach, Hardware based speculation, ILP using multiple issue and static scheduling, ILP using dynamic scheduling-case study- Intel Core i7. Data level parallelism-Vector Architecture, Graphic processing unit, Centralized shared memory architecture, Multiprocessor cache coherence - Distributed shared memory, Schemes for enforcing coherence Interconnection Network Design, Designing Multicore Architectures -- Unique challenges in multicore architectures

Expected Outcome

The students will be to

1. Know design issues of processors and performance measurement of processors
2. Apply instruction level parallelism and data Level Parallelism
3. Understand Multiprocessor systems, cache coherence and Interconnection networks

Text Books

1. D.E. Culler, J.P. Singh, and A. Gupta. Parallel Computer Architecture - A Hardware/Software Approach. Morgan Kaufmann Publishers, 2010.
2. Hennessy J. L., D. Patterson, “Computer Architecture – A quantitative Approach”, 5/e, Morgan Kauffman 2012.

References

1. Kai Hwang, “Advanced Computer Architecture Parallelism, Scalability, Programmability”, Tata McGraw-Hill, 2003.
2. Research papers from top conferences such as ISCA, HPCA, MICRO, and ASPLOS.
3. S.W. Keckler, K. Olukotun, and H.P. Hofstee. Multicore Processors and Systems. Springer, 2009.
4. W.J. Dally and B. Towles. Principles and Practices of Interconnection Networks. Morgan Kaufmann Publishers, 2003.
5. WWW Computer Architecture page. http://www.cs.wisc.edu/arch.

Course Plan

Module	Contents	Hours	Sem. Exam Marks

www.ktubtechquestions.com

I	Computer architecture - design issues-Memory wall, Power Wall , Frequency Wall Classes of parallelism and parallel architecture,	**4**	**15%**
	Performance measurements, Pipelining- Scalar and super scalar processors- Instruction level parallelism -concepts and challenges, ILP Wall	**4**	
II	Data hazards, Structural Hazards, Branch Hazards, Branch Prediction schemes	**4**	**15%**
	Basic compiler techniques for exposing instruction-level parallelism.	**4**	
FIRST INTERNAL EXAM			
III	Dynamic Scheduling- Tomasulo's approach, Hardware based speculation.	4	15%
	ILP using multiple issue and static scheduling, ILP using dynamic scheduling, multiple issue and speculation.	**4**	
IV	Case study- Intel Core i7.	**4**	**15%**
	Data level parallelism-Vector architecture-Vector instruction types, Vector-Access memory schemes , Graphic processing units.	**4**	
SECOND INTERNAL EXAM			
V	Centralized shared memory architecture. Multiprocessor cache coherence Distributed shared memory and Directory based coherence.	**4**	**20%**
	Interconnection Network Design -- Interconnection topologies, routing techniques, flow control mechanisms, router architecture, arbitration logic	**4**	
VI	Designing Multicore Architectures -- Unique challenges in multicore architectures,	**4**	**20%**
	Multicore memory hierarchy organization, dealing with performance volatility, multicore memory traffic reduction techniques.	**4**	
END SEMESTER EXAM			

QUESTION PAPER PATTERN

Maximum Marks: 100 Exam Duration: 3 hours

The question paper shall consist of Part A, Part B and Part C.

Part A shall consist of three questions of 15 marks each uniformly covering Modules I and II. The student has to answer any two questions (15×2=30 marks).

Part B shall consist of three questions of 15 marks each uniformly covering Modules III and IV. The student has to answer any two questions (15×2=30 marks).

Part C shall consist of three questions of 20 marks each uniformly covering Modules V and VI. The student has to answer any two questions (20×2=40 marks).

Note : Each question can have a maximum of 4 subparts, if needed