Course code	Course Name	L-T-P-Credits	Year of Introduction
IC365	DESIGN OF DIGITAL SYSTEMS	3-0-0-3	2016

Prerequisite: Nil

Course Objectives

- To study hazards in combinational and sequential circuits
- To review the fundamentals of finite state machines
- To study asynchronous sequential circuits
- To study various programmable logic devices
- To study the fundamentals of VHDL programming

Syllabus

Hazards – Clock skew – synchronizer failure and metastability – finite state machines – asynchronous sequential circuits, analysis and synthesis – designing with programmable logic devices: ROM, PAL, PLA, CPLD and FPGA devices - Introduction to VHDL programming.

Expected Outcome

After the completion of the course, students will be able to

i. Explain hazards in combinational and sequential circuits
ii. Design and implement synchronous sequential circuits
iii. Analyse and synthesise asynchronous sequential circuits
iv. Draw and explain architecture of important PLDs
v. Program simple digital circuits using VHDL

Text Book

- John F Wakerly, Digital Design- Principles and Practices(Third edition), Pearson

References

1. Bhasker J, A VHDL Primer, Addison Wesly.
2. Kevin Skahill 'VHDL for Programmable Logic' Pearson Education
3. Perry D.L, VHD, McGraw Hill
4. Roth C.H.Jr., Digital system Design using VHDL, PWS Pub.co
5. Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with VHDL Design, TMH

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	Hazards - Static and Dynamic hazards- Design of hazard free circuits. Elementary ideas of Clock skew, synchronizer failure and metastability Review of synchronous sequential circuit design using finite state machines – Mealy & Moore Machines - ASM charts	8	15%

II	Asynchronous sequential circuits: Asynchronous behavior- Analysis of asynchronous circuits- Synthesis of asynchronous circuits- Race condition- State reduction- State assignment- Transition diagrams	8	**15%**
FIRST INTERNAL EXAM			
III	Designing with Programmable devices: ROM - Programmable Logic Arrays- Programmable Array Logicsequential-combinational PLDs (Eg: PAL14L4 &PAL12H6)	5	**15%**
IV	Sequential PLDs (Eg: PAL16R4)- Simple PLDs (Eg: 22V10)- Complex Programmable Logic Devices (Eg: XC9500)- Field Programmable Gate Arrays (Eg: XC 4000 & FLEX 10K)	7	**15%**
SECOND INTERNAL EXAM			
V	Introduction to VHDL: Entities and architectures- Behavioural, Data flow and structural descriptions- Identifies, Data objects, Data types and attributes- Delay models- Delta delays	7	**20%**
VI	VHDL codes for simple combinational and sequential circuits- State Machine Design, simple examples- Sub programs and packages	7	**20%**
END SEMESTER EXAM			

QUESTION PAPER PATTERN:

Maximum Marks: 100 Exam Duration: 3 Hours

Part A

Answer any two out of three questions uniformly covering Modules 1 and 2. Each question carries 15 marks and can have not more than four sub divisions. (15 x 2 = 30 marks)

Part B

Answer any two out of three questions uniformly covering Modules 3 and 4. Each question carries 15 marks and can have not more than four sub divisions. (15 x 2 = 30 marks)

Part C

Answer any two out of three questions uniformly covering Modules 5 and 6. Each question carries 20 marks and can have not more than four sub divisions. (20 x 2 = 40 marks)