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Course code	Course Name	L-T-P-Credits	Year of Introduction
IC303	MICROPROCESSORS	3-0-0-3	2016

Prerequisite : Nil

Course Objectives

- To understand the architecture of a microprocessor
- To know interfacing memory with a microprocessor
- To know interfacing various peripherals, analog and digital devices with a microprocessor
- To understand the basic concepts and elements of architecture of advanced microprocessors.

Syllabus

Architecture of Intel 8086 microprocessor- Interfacing memory, peripheral chips and input output devices to 8086- Basic concepts and architectures of advanced microprocessors.

Expected Outcome

After the completion of the course, students should be able to

- Comprehend systems built around microprocessors.
- Effectively utilize systems built around microprocessors in industry for various purposes
- Keep in pace with the advances in microprocessor industry

Text Book:

- A.K Ray and K.M. Bhurchandi, Advanced Microprocessors and Peripherals, McGraw Hill Education, 3e

References:

1. Douglas V. Hall, Microprocessors and Interfacing, McGraw Hill Education, 3e
2. Liu and Gibson, Microprocessor systems, the 8086/8088 family: Architecture, programming and Design, Prentice Hall of India, 2e
3. Lyla B. Das, The x86 Microprocessors, Pearson, 2e
4. INTEL and AMD websites

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	Evolution of microprocessors - Architecture of Intel 8086- Execution Unit and Bus interface Unit-Memory segmentation- Addressing modes of of 8086-Illustrative examples using simple instructions	7	15%
II	Signal descriptions of Intel 8086/8088-Building basic minimum and maximum mode systems- Timing diagrams	6	15%
FIRST INTERNAL EXAM			

III	Stack organisation of 8086-Interrupt system of 8086 –types of interrupts- Basic concepts of BIOS and DOS interrupts	3	**15%**
	Intel 8259 Interrupt Controller and its interfacing with 8086. Programmable Peripheral Interface (8255) and its interface with 8086/8088. DMA-Interfacing DMA controller to 8086	4	
IV	Interfacing multiplexed LED displays with 8086-Intel 8254 Timer and its interfacing- Intel 8279 display/keyboard controller and its interfacing- -Serial Communication-RS 232C interface-Intel 8251 USART. Interfacing static RAM and ROM to 8086/8088- Introduction to DRAMs	7	**15%**
	SECOND INTERNAL EXAM		
V	A brief description of the architecture of Pentium Processor - Real and Protected Modes- memory management system in protected mode- Concepts of virtual memory, Descriptor Tables, privilege levels and protection, Paging- Basic concept of Net Burst Architecture	8	**20%**
VI	Important RISC concepts-Pipe lining-Different types of caches - Branch Prediction and Translation Look Aside Buffer, Out of order Execution, RISC and CISC convergence- Basic concepts of multi-core architecture- *An overview of the recent advances in microprocessor industry.*	7	**20%**
	END SEMESTER EXAM		

QUESTION PAPER PATTERN:

Maximum Marks: 100 Exam Duration: 3 Hours

Part A

Answer any two out of three questions uniformly covering Modules 1 and 2. Each question carries 15 marks and can have not more than four sub divisions. (15 x 2 = 30 marks)

Part B

Answer any two out of three questions uniformly covering Modules 3 and 4. Each question carries 15 marks and can have not more than four sub divisions. (15 x 2 = 30 marks)

Part C

Answer any two out of three questions uniformly covering Modules 5 and 6. Each question carries 20 marks and can have not more than four sub divisions. (20 x 2 = 40 marks)