

Course code	Course Name	L-T-P - Credits	Year of Introduction
EE363	Computer Organization and Design	3-0-0-3	2016
Prerequisite: Nil			
Course Objectives			
<ul style="list-style-type: none"> To lay the foundation for the study of hardware organization of digital computers. To impart the knowledge on interplay between various building blocks of computer 			
Syllabus			
Basic operational concepts, CPU structure, Arithmetic, Memory hierarchy, Input Output interfacing, Performance analysis, Design			
Expected outcome.			
<ul style="list-style-type: none"> The students will gain general idea about the functional aspects of each building blocks in computer design 			
Text Book:			
W. Stallings, Computer Organization and Architecture: Designing for Performance, 8 th Ed., Pearson Education India.			
References:			
<ol style="list-style-type: none"> D. A. Patterson and J. L. Hennessy, Computer Organization and Design, 4th Ed., Morgan Kaufmann, 2008. Hamacher, Vranesic & Zaky, Computer Organization, McGraw Hill Heuring V. P. & Jordan H. F., Computer System Design & Architecture, Addison Wesley 			
Course Plan			
Module	Contents	Hours	Sem. Exam Marks
I	Basic Structure of computers – functional units – Historical Perspective -Basic operational concepts – bus structures, Measuring performance: evaluating, comparing and summarizing performance	7	15%
II	Memory locations and addresses – memory operations – instructions and instruction sequencing ,Instruction sets- RISC and CISC paradigms, Addressing modes	7	15%
FIRST INTERNAL EXAMINATION			
III	Computer arithmetic - Signed and unsigned numbers - Addition and subtraction - Logical operations - Constructing an ALU - Multiplication and division – faster versions of multiplication- floating point representation and arithmetic	7	15%
IV	The processor: Building a data path - Simple and multi-cycle implementations - Microprogramming – Exceptions	6	15%
SECOND INTERNAL EXAMINATION			
V	Introduction to pipelining-pipeline Hazards, Memory hierarchy - Caches - Cache performance - Virtual memory - Common framework for memory hierarchies	7	20%
VI	Input/output - I/O performance measures – I/O techniques - interrupts, polling, DMA; Synchronous vs. Asynchronous I/O; Controllers. Types and characteristics of I/O devices - Buses - Interfaces in I/O devices - Design of an I/O system	8	20%
END SEMESTER EXAM			

QUESTION PAPER PATTERN:

Maximum Marks: 100

Exam Duration: 3Hours.

Part A: 8 compulsory questions.

One question from each module of Module I - IV; and two each from Module V & VI.

Student has to answer all questions. $(8 \times 5) = 40$

Part B: 3 questions uniformly covering Modules I & II. Student has to answer any 2 from the 3 questions: $(2 \times 10) = 20$. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

Part C: 3 questions uniformly covering Modules III & IV. Student has to answer any 2 from the 3 questions: $(2 \times 10) = 20$. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

Part D: 3 questions uniformly covering Modules V & VI. Student has to answer any 2 from the 3 questions: $(2 \times 10) = 20$. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

