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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JUNE 2017

Course Code: **EE 204**

Course Name: **DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)**

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 5 marks

1. (a) Create a table showing 4 – bit Gray Code and the corresponding Binary Code. Explain how the table is derived. (5)
2. Using K – Map derive the reduced Boolean expression for the following function.
$$f(A, B, C, D) = \sum m(0,1,3,4,6,9,11) + d(2,5)$$ (5)
3. Draw the truth table for a full subtractor. Reduce it using K – Map. Implement it using logic gates. (5)
4. Realize a J K Master Slave flip flop using NAND gates. Explain its working (5)
5. Differentiate between Asynchronouscounters and Svnchronous counters with the help of diagrams. What are the advantages and disadvantages ? (5)
6. Design a 4 bit Ring counter . Draw the Truth Table and the waveform. (5)
7. Analyse the working of a R- 2R ladder Digital to analog converter with the help of a diagram. (5)
8. Design a Full Adder using VHDL. (5)

PART B

Answer any two questions. Each carries 10 marks.

9. (a) Differentiate between the methods of binary subtraction using 1's complement and 2'scomplement. Show an example in each case with 4 bit numbers. (6)
(b) Determine the range of numbers in 1's complement and 2's compliment for word length of 8 bit and 16 bit. (4)
10. (a) Simplify using K – Map.
$$F(A, B, C, D) = \prod M(1, 3, 5, 7, 13, 15)$$ (6)
(b) State and prove De Morgan's theorem. (4)

11. (a) Express the following function as a sum of minterms.
$$F(A, B, C, D) = B'D + A'D + BD$$ (6)
(b) Draw the circuit diagram of a typical TTL gate and explain. (4)

PART C

Answer any two questions. Each question carries 10 marks.

12. Describe the working of a Carry Look Ahead Adder using the example of 4 – bit numbers. Clearly show the derivations of the equations. Show the implementation in Hardware. (10)
13. (a) Realize the following function using 4×1 multiplexer.
$$F(A, B, C) = \sum m(1, 3, 5, 6)$$ (5)
(b) Design a BCD to Decimal decoder. Write down the Truth Table, Boolean expressions and show the Hardware implementation. (5)
14. (a) Draw a 4 – bit Asynchronous up counter and discuss its characteristics. Draw the waveforms. (5)
(b) Draw a 4 – bit Serial-In-Parallel-Out shift register and explain its working. (5)

PART D

Answer any two questions. Each question carries 10 marks.

15. Design a Mod 6 Synchronous counter. Enumerate all the steps in the design. (10)
16. (a) Design a two bit flash type analog to digital converter. Explain its working. (6)
(b) Compare and contrast between ROM, PROM and EPROM. (4)
17. Describe the structure of a Programmable logic array. Take a simple example and explain. (10)