COURSE CODE	COURSE NAME	L-T-P-C	YEAR OF INTRODUCTION
EC 361	DIGITAL SYSTEM DESIGN	3-0-0-3	2015

Prerequisite: EC207 Logic Circuit Design

Course objectives:

The purpose of this course is:

5. To study synthesis and design of CSSN
6. To study synthesis and design of ASC
7. To study hazards and design hazard free circuits
8. To study PLA folding
9. To study architecture of one CPLDs and FPGA family

Syllabus:

Clocked synchronous networks, asynchronous sequential circuits, Hazards, Faults, PLA, CPLDs and FPGA

Expected outcome:

The student should able:

1. To analyze and design clocked synchronous sequential circuits
2. To analyze and design asynchronous sequential circuits
3. To apply their knowledge in diagnosing faults in digital circuits, PLA
4. To interpret architecture of CPLDs and FPGA

Text Books:

1. Donald G Givone, Digital Principles & Design, Tata McGraw Hill, 2003
2. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning
3. John F Wakerly, Digital Design, Pearson Education, Delhi 2002

References:

1. Richard E. Haskell, Darrin M. Hanna , Introduction to Digital Design Using Digilent FPGA Boards, LBE Books- LLC
2. N. N. Biswas, Logic Design Theory, PHI
3. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, Digital Systems Testing and Testable Design, John Wiley & Sons Inc.
4. Z. Kohavi, Switching and Finite Automata Theory, 2nd ed., 2001, TMH
5. Morris Mano, M.D.Ciletti, Digital Design, 5th Edition, PHI.
6. Samuel C. Lee, Digital Circuits and Logic Design, PHI

Course Plan

Module	Course content	Hours	Sem. Exam Marks
I	Analysis of clocked Synchronous Sequential Networks(CSSN)	2	15
	Modelling of CSSN – State assignment and reduction	1	
	Design of CSSN	2	
	Iterative circuits	1	
	ASM Chart and its realization	2	
II	Analysis of Asynchronous Sequential Circuits (ASC)	2	15
	Flow table reduction- Races in ASC	1	
	State assignment problem and the transition table- Design of AS	2	
	Design of Vending Machine controller.	2	

FIRST INTERNAL EXAM			
III	Hazards – static and dynamic hazards – essential	1	**15**
	Design of Hazard free circuits – Data synchronizers	1	
	Mixed operating mode asynchronous circuits	1	
	Practical issues- clock skew and jitter	1	
	Synchronous and asynchronous inputs – switch bouncing	2	
IV	Fault table method – path sensitization method – Boolean difference method	2	**15**
	Kohavi algorithm	2	
	Automatic test pattern generation – Built in Self Test(BIST)	3	
SECOND INTERNAL EXAM			
V	PLA Minimization - PLA folding	2	**20**
	Foldable compatibility Matrix- Practical PLA	2	
	Fault model in PLA	1	
	Test generation and Testable PLA Design.	3	
VI	CPLDs and FPGAs - Xilinx XC 9500 CPLD family, functional block diagram– input output block architecture - switch matrix	3	**20**
	FPGAs – Xilinx XC 4000 FPGA family – configurable logic block - input output block, Programmable interconnect	3	
END SEMESTER EXAM			

Question Paper Pattern

The question paper consists of three parts. Part A covers modules I and II, Part B covers modules III and IV and Part C covers modules V and VI. Each part has three questions. Each question has a maximum of four subparts. Among the three questions one will be a compulsory question covering both the modules and the remaining two questions will be as one question from each module, of which one is to be answered. Mark pattern is according to the syllabus with 50 % for theory, derivation, proof and 50% for logical/numerical problems.