<table>
<thead>
<tr>
<th>Course No.</th>
<th>Course Name</th>
<th>L-T-P-Credits</th>
<th>Year of Introduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS203</td>
<td>Switching Theory and Logic Design</td>
<td>3-1-0-4</td>
<td>2016</td>
</tr>
</tbody>
</table>

Pre-requisite: Nil

**Course Objectives**
1. To impart an understanding of the basic concepts of Boolean algebra and digital systems.
2. To impart familiarity with the design and implementation of different types of practically used sequential circuits.
3. To provide an introduction to use Hardware Description Language

**Syllabus**

**Expected Outcome:**
Students will be able to:
1. apply the basic concepts of Boolean algebra for the simplification and implementation of logic functions using suitable gates namely NAND, NOR etc.
2. design simple Combinational Circuits such as Adders, Subtractors, Code Convertors, Decoders, Multiplexers, Magnitude Comparators etc.
3. design Sequential Circuits such as different types of Counters, Shift Registers, Serial Adders, Sequence Generators.
4. use Hardware Description Language for describing simple logic circuits.
5. apply algorithms for addition/subtraction operations on Binary, BCD and Floating Point Numbers.

**Text Books:**
1. Mano M. M., *Digital Logic & Computer Design*, 4/e, Pearson Education, 2013. [Chapters: 1, 2, 3, 4, 5, 6, 7].

**References:**

**COURSE PLAN**

<table>
<thead>
<tr>
<th>Module</th>
<th>Contents</th>
<th>Contact Hours (52)</th>
<th>Sem. Exam Marks;%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| I | Number systems – Decimal, Binary, Octal and Hexadecimal – conversion from one system to another – representation of negative numbers – representation of BCD numbers – character representation – character coding schemes – ASCII – EBCDIC etc.  
Addition, subtraction, multiplication and division of binary numbers (no algorithms). Addition and subtraction of BCD, Octal and Hexadecimal numbers.  
Representation of floating point numbers – precision – addition, subtraction, multiplication and division of floating point numbers | 10 | 15% |
| II | Introduction — Postulates of Boolean algebra – Canonical and Standard Forms — logic functions and gates  
methods of minimization of logic functions — Karnaugh map method and QuinMcClusky method  
Product-of-Sums Simplification — Don’t-Care Conditions. | 09 | 15% |
| III | Combinational Logic: combinational Circuits and design Procedure — binary adder and subtractor — multi—level NAND and NOR circuits — Exclusive-OR and Equivalence Functions.  
Implementation of combination logic: parallel adder, carry look ahead adder, BCD adder, code converter, magnitude comparator, decoder, multiplexer, de-multiplexer, parity generator. | 10 | 15% |
Clocked sequential circuits: state diagram — state reduction and assignment — design with state equations | 08 | 15% |
Counters: asynchronous counters — binary and BCD ripple counters — timing sequences — synchronous counters — up-down counter, BCD counter, Johnson counter — timing sequences and state diagrams. | 08 | 20% |
### Question Paper Pattern:

1. There will be five parts in the question paper – A, B, C, D, E
2. **Part A**
   - Total marks: 12
   - Four questions each having 3 marks, uniformly covering module I and II; All four questions have to be answered.
3. **Part B**
   - Total marks: 18
   - Three questions each having 9 marks, uniformly covering module I and II; Two questions have to be answered. Each question can have a maximum of three subparts
4. **Part C**
   - Total marks: 12
   - Four questions each having 3 marks, uniformly covering module III and IV; All four questions have to be answered.
5. **Part D**
   - Total marks: 18
   - Three questions each having 9 marks, uniformly covering module III and IV; Two questions have to be answered. Each question can have a maximum of three subparts
6. **Part E**
   - Total Marks: 40
   - Six questions each carrying 10 marks, uniformly covering modules V and VI; four questions have to be answered.
   - A question can have a maximum of three sub-parts.
7. There should be at least 60% analytical/design/numerical questions.